intervening curing or partial curing step is required and, accordingly, the types of encapsulation material that can be employed according to the invention is not limited to ones that are suitable for a two-stage cure. Because the chip carries the limited quantity of encapsulant material, the encapsulation is self-aligned as the chip and the substrate are brought together during bonding.

The specific points raised by the Examiner will now be addressed, beginning with objections to the specification.

Objections to the specification

The specification was objected to because of certain informalities, and appropriate correction was required. Paragraph [0012] is amended herein to rewrite "applying precise" as -- applying a precise -- (page 3, line 15), and to rewrite "measure volume" as -- measured volume -- (page 3, line 21), and the objection may now be withdrawn as to these informalities.

However, no change is made to insert -- an -- before "apparatus" either in "features apparatus" (page 3, line 15) or in "Also, apparatus" (Abstract, 10th line), as suggested by the Examiner. Applicant respectfully submits that such "correction" would not be appropriate. The usage of the word "apparatus" without an article, as here, is entirely accepted in U.S. patent practice; among other things, this conveys the meaning of "apparatus" in either singular or plural form. Applicant respectfully requests that the objection as to "apparatus" be withdrawn.

Rejection under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Yamaji U.S. 5,925,936 ("Yamaji"); and claim 1 was rejected under 35 U.S.C. § 102(e) as being anticipated by Witzman *et al.* U.S. 6,037,192 ("Witzman"), or by Chino *et al.* U.S. 6,184,066 B1 ("Chino"), or by Capote *et al.* U.S. 6,297,560 B1 ("Capote").

As to Yamaji the Examiner stated:

> Yamaji teaches a method of encapsulating flip chip interconnects. A quantity of thermoplastic resin 3 is disposed upon the active side of a chip 5. The resin 3 surrounds the connection electrodes 4 as shown in figure 3A. After the resin 4 has been applied to the chip 5, the chip is bonded to a mounting substrate 6, wherein the

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> connection electrodes 4 attach to substrate electrodes (bonding pads) 7.

As to Witzman the Examiner stated:

> Weitzman et al. teach a method of encapsulating flip chip interconnects, as shown in figures 3 and 4. In figure 3, a quantity of polymer adhesive (resin) 18 is applied to components (chips) 20. The adhesive is applied to the side of the components having interconnects 22. After the polymer adhesive 18 is applied to the components 20, the components 20 are bonded to substrates 10, wherein the substrates 10 poses conductors 12 and solderable pads (bonding pads) 16. The interconnects 22 of the component directly c0ntact the solderable pads 16 to effect the electrical connection.

As to Chino the Examiner stated:

> Chino et al. teach a method of encapsulating flip chip interconnects. The method, as described in column 1, lines 60-67 and continued to column 2, lines 6-8, includes applying a resin to either the semiconductor chip or the substrate to which the chip will be mounted.

As to Capote the Examiner stated:

> Capote et al. teach a method of encapsulating flip chip interconnects. As shown in figure 4, solder bumps (interconnects) 14 on the active side of a chip 10 are coated in encapsulant material (resin) 22. After the application of the encapsulant 22, the chip 10 is bonded to a substrate 20, such that the solder bumps 14 of the chip 10 electrically connect to solder pads (bonding pads) 12 of the substrate 20.

These rejections are respectfully traversed. Each of the cited patents differs from, and none discloses, Applicant's invention.

Yamaji describes completely covering the top and side surfaces of the bump electrodes with a thermoplastic resin, then polishing the resin and bump electrodes parallel with the wafer surface to expose a contact surface of the bump. Then the chip is mounted on the substrate with the bump electrode surfaces in contact with the respective substrate electrodes, and the assembly is placed in a furnace for reflow to effect the electrical connection. According to Yamaji the resin has a glass transition temperature equal to or less than the melting temperature of the material used in the terminal-to-terminal connection, so that during reflow the resin becomes molten to bond the

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resin to the substrate. Yamaji does not describe or suggest applying a limited quantity of encapsulant material to the bumps on the chip, as in Applicant's invention. Nor does Yamaji describe or suggest displacement of encapsulant material from between the respective bumps and pads during bonding, as in Applicant's invention. Accordingly the rejection of claim 1 over Yamaji can be withdrawn.

Witzman describes, in a first embodiment, applying encapsulant to the substrate, and not to the component. In a second embodiment Whitman describes applying the encapsulant to an entire wafer in an inverted position (terminals upward) and partially curing the encapsulant to form a solid state matrix prior to singulation, then simulating the components, inverting the components on the substrate, and completing the cure during high temperature reflow. Witzman does not describe or suggest applying a limited quantity of encapsulant material to the bumps on the chip, and curing the encapsulant after forming the bump-to-pad interconnect, as in Applicants' invention. Accordingly the rejection of claim 1 over Witzman can be withdrawn.

Chino describes mounting a laser chip onto a silicon submount by applying a UV curable resin onto the submount and then pressing the laser chip into the resin. Chino does not show forming a flip chip interconnect by applying encapsulant material onto bumps on the interconnect surface of the chip and then contacting the chip with the substrate, as in Applicant's invention. Accordingly the rejection of claim 1 over Chino can be withdrawn.

Capote describes forming a flip chip attachment by (referring to Fig. 4) precoating the chip with an underfill material patterned so that the "discrete solder bumps" have the "encapsulant material therearound"; that is, the encapsulant is put "between the solder bumps". (Col. 6, lines 53 - Col. 7, line 3). In one embodiment the solder bumps protrude beyond the encapsulant; in an alternate embodiment the solder bumps are covered by the encapsulant and the encapsulant is subsequently removed to expose the solder bumps prior to attachment and reflow. (Col. 7, lines 3 - 16). Accordingly the rejection of claim 1 over Capote can be withdrawn.

Accordingly, it is submitted that neither Yamaji nor Witzman nor Chino nor Capote teaches or suggests Applicants' invention as claimed, and the rejections of claim 1 for anticipation should now be withdrawn. Nor does any combination of any of Yamaji, Witzman, Chino, and Capote teach or suggest Applicants' invention.

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Claims 2 - 7 were deemed allowable, but were objected to as depending from rejected claim 1. In view of the foregoing, it is believed that claim 1 is allowable and, accordingly, that claims 1 - 7 are in condition for allowance; and action to that effect is requested.

Newly added claims 12 - 17 are directed to "allowable subject matter" as deemed by the Examiner; that is, claims 12 - 17 track the language of claims 2 - 7, claims 12 and 15 being written in independent form including all the recitations of base claim 1 as originally filed. Accordingly, it is believed that claims 12 - 17 are in condition for allowance, and action to that effect is requested.

This Amendment is being filed within the second month followed shortened statutory period set by the Examiner, and it is accompanied by a petition for two months' extension of time and a fee or fee authorization therefor. If the Examiner determines that a further extension of time is required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge the fee to Deposit Account 50-0869 (Order No. CPAC 1011-2).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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Attachment under Rule 1.121
(Specification)

The paragraph beginning at line 15 on page 3 (paragraph 0012) is amended as follows:

In another general aspect the invention features apparatus for applying a precise volume of encapsulating resin to a chip, including a reservoir having a bottom, and means for dispensing a pool of encapsulating resin to a predetermined depth over the reservoir bottom. In some embodiments the reservoir is at least deep enough to accommodate a pool having a predetermined depth that approximates a bump standoff height on the chip. In some embodiments the means for dispensing the resin pool includes means for dispensing a [measure] measured volume of resin into the reservoir. In some embodiments the means for dispensing the resin pool includes means for dispensing an excess of resin into the reservoir, and means such as a doctor for removing the excess; in such embodiments the predetermined depth of the pool is established by the depth of the reservoir itself.

The paragraph beginning at line 27 on page 4 (paragraph 0019) is amended as follows:

FIG. **3** shows a chip **10** that has been withdrawn from a resin pool. Evidently, the interconnect side of the chip shown in FIG. **3** was dipped to a greater depth in a resin pool [and] than is shown in FIG. **2**, inasmuch as in FIG. **3** the resin mass **34** is shown as being carried not only on the bumps **16** but also on the surface **17** of the semiconductor die. As will be appreciated, the quantity of resin in a resin mass carried by the chip after the chip is withdrawn from the resin pool will depend not only upon the extent of contact to the chip with the resin in the pool, but also upon surface characteristics (for example, wettability by the resin) of the various features on the chip and upon characteristics (for example, viscosity) of the resin itself. A desired predetermined depth to which a particular chip should be dipped in a particular resin composition, to result in a particular desired encapsulation form, can readily be determined without undue experimentation. FIG. **3** also shows a package substrate **40** having metal interconnect pads **42** in an arrangement complementary to the arrangement of the bumps on the chip, and the tool **12** is holding the chip in apposition to the substrate with the corresponding bumps and pads aligned. The tool is poised in FIG. **3** to bring the chip and substrate together as shown for example in FIG. **4**.

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Attachment under Rule 1.121
(Claims)

1. (Amended) A method for encapsulating flip chip interconnects, comprising [comprises] applying a limited quantity of encapsulating resin to at least interconnect bumps on an [the] interconnect side of [an] a singulated integrated circuit chip, and thereafter bringing the chip together with a substrate under conditions that result in displacement of encapsulant from between the [promote the bonding of] bumps on the interconnect side of the chip [with] and respective bonding pads on the substrate, and that promote the bonding of bumps with the respective pads.

2. (Amended) The method of claim 1 wherein the step of applying resin to the chip comprises dipping the bumps on the interconnect side of the chip to a predetermined depth in a pool of resin, and then withdrawing the chip from the resin pool.

3. (Unchanged) The method of claim 2 wherein the predetermined depth to which the chip is dipped in the pool approximates a bump standoff height, so that the surface of the resin pool contacts a surface of the chip, so that as the chip is withdrawn from the resin pool some quantity of resin may remain on the chip surface as well as on features that standoff from the chip surface.

4. (Unchanged) The method of claim 2 wherein the predetermined depth to which the chip is dipped in the pool is less than the bump standoff height, so that the chip surface does not contact the resin pool, with the result that when the chip is withdrawn from the resin pool some quantity of resin remains only on features that standoff from the chip surface.

5. (Amended) The method of claim 1 wherein applying resin to the chip comprises providing a reservoir having a bottom, providing a pool of resin in the reservoir to a shallow depth over the reservoir bottom, dipping the bumps on the chip into the resin pool so that bumps on the chip contact the reservoir bottom, and then withdrawing the chip from the resin pool.

6. (Unchanged) The method of claim 5 wherein the shallow depth of the pool over the reservoir bottom approximates the bump standoff height.

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7. (Unchanged) The method of claim 5 wherein the shallow depth of the pool over the reservoir bottom is less than the standoff height.

12. (New) A method for encapsulating flip chip interconnects, comprising applying a limited quantity of encapsulating resin to the interconnect side of an integrated circuit chip by dipping the interconnect side of the chip to a predetermined depth in a pool of resin and then withdrawing the chip from the resin pool, and thereafter bringing the chip together with a substrate under conditions that promote the bonding of bumps on the interconnect side of the chip with bonding pads on the substrate.

13. (New) The method of claim 12 wherein the predetermined depth to which the chip is dipped in the pool approximates a bump standoff height, so that the surface of the resin pool contacts a surface of the chip, so that as the chip is withdrawn from the resin pool some quantity of resin may remain on the chip surface as well as on features that standoff from the chip surface.

14. (New) The method of claim 12 wherein the predetermined depth to which the chip is dipped in the pool is less than the bump standoff height, so that the chip surface does not contact the resin pool, with the result that when the chip is withdrawn from the resin pool some quantity of resin remains only on features that standoff from the chip surface.

15. (New) A method for encapsulating flip chip interconnects, comprising applying a limited quantity of encapsulating resin to the interconnect side of an integrated circuit chip by providing a reservoir having a bottom, providing a pool of resin in the reservoir to a shallow depth over the reservoir bottom, dipping the chip into the resin pool so that bumps on the chip contact the reservoir bottom, and then withdrawing the chip from the resin pool; and thereafter bringing the chip together with a substrate under conditions that promote the bonding of bumps on the interconnect side of the chip with bonding pads on the substrate.

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16. (New) The method of claim 15 wherein the shallow depth of the pool over the reservoir bottom approximates the bump standoff height.

17. (New) The method of claim 15 wherein the shallow depth of the pool over the reservoir bottom is less than the standoff height.

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